(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号

特開2001－67133

（P2001－67133A）

(43)公開日　平成13年３月16日(2001.3.16)

(51)Int.Cl.⁷	識別記号	ＦＩ	テーマコード（参考）
Ｇ０５Ｆ　1/618	３１０	Ｇ０５Ｆ　1/618　３１０	５Ｃ００６
Ｇ０９Ｇ　3/36		Ｇ０９Ｇ　3/36	５Ｈ４３０

審査請求　未請求　請求項の数１　ＯＬ　（全　６　頁）

(21)出願番号　特願平11－242509

(22)出願日　平成11年８月30日(1999.8.30)

(71)出願人　000116024
ローム株式会社
京都府京都市右京区西院溝崎町21番地

(72)発明者　田中　寿昌
京都市右京区西院溝崎町21番地　ローム株式会社内

(74)代理人　100083231
弁理士　紋田　誠　（外１名）

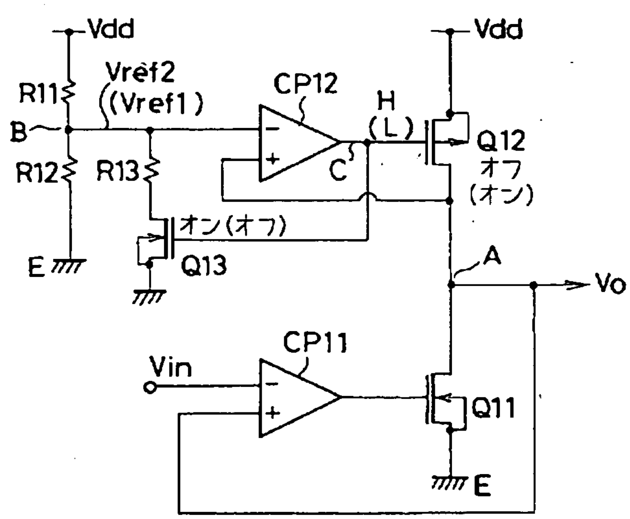
Ｆターム(参考)　5C006 AF51 BF14 BF25 BF32 BF43
FA31 FA47
5H430 BB03 BB09 BB11 EE06 EE07
FF01 FF13 GG05 HH03 HH07

(54)【発明の名称】　電源回路

(57)【要約】

【課題】　ボルテージフォロワの出力段を構成する電源回路において、出力電圧へのノイズ成分の除去能力を向上し、容量性負荷の駆動能力を大きくすると共に、低消費電力化も合わせて達成する。

【解決手段】　電源間に第１スイッチング素子Ｑ１１と第２スイッチング素子Ｑ１２を設ける。入力電圧Ｖｉｎと出力電圧Ｖｏとを比較ＣＰ１１し、この出力電圧Ｖｏが入力電圧Ｖｉｎを上回るときに、第１スイッチング素子Ｑ１１を導通させる。また、参照電圧Ｖｒｅｆと出力電圧Ｖｏとを比較ＣＰ１２し、この出力電圧Ｖｏが前記参照電圧Ｖｒｅｆを下回るときに、前記第２スイッチング素子Ｑ１２を導通させる。この差動増幅器ＣＰ１２の動作にヒステリシス特性を持たせる。



【特許請求の範囲】

【請求項1】　出力端子と第1電源間に接続された第1スイッチング素子と、
第2電源と前記出力端子間に接続された第2スイッチング素子と、
入力電圧と前記出力端子の出力電圧とを比較し、この出力電圧が入力電圧を上回るときに、前記第1スイッチング素子を導通させる第1比較器と、
参照電圧と前記出力電圧とを比較し、この出力電圧が前記参照電圧を下回るときに、前記第2スイッチング素子を導通させる第2比較器とを備え、
該第2比較器の動作にヒステリシス特性を持たせたことを特徴とする電源回路。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、設定された電圧をインピーダンス変換して出力する電源回路、特に複数の電圧を必要とする液晶表示装置に好適な電源回路に関する。

【0002】携帯電話やページャなどの携帯機器用の表示装置として、液晶表示装置が使用されている。液晶表示装置では、複数のバイアス電圧を用いてデューティ駆動する図5に示すような駆動回路が用いられ、多くの表示素子を駆動できるようにしている。

【0003】図5の液晶表示装置は、電源電圧Ｖｄｄと接地電圧Ｅとの間に、直列に接続された各々１ＭΩ程の抵抗で分圧して複数のバイアス電圧を発生するバイアス回路部５１と、発生された各バイアス電圧をインピーダンス変換して出力するためのボルテージフォロワ５２１～５２３を有するバッファ回路部５２と、バッファ回路部の出力電圧を表示データなどに応じて点灯すべき液晶表示素子５４１の電極に選択して印加するための選択回路部５３と、複数の液晶表示素子５４１から表示パターンが形成される表示パネル部５４から構成されている。

【0004】そして、複数のバイアス電圧によるデューティ駆動を行うことにより、表示パネル部５４上の多数の液晶表示素子の電極間に印加された電圧が所定値以上のもののみを点灯表示することができる。

【0005】このように構成された液晶表示装置では、特に使用時間をできるだけ長くするために低消費電力化と、負荷容量が大きい場合にも駆動波形の鈍化を防止し表示品位を保つために容量性負荷を駆動する駆動力の向上が必要である。

【0006】このため、従来、バッファ回路部のボルテージフォロワの出力段を構成する電源回路として、図６，図7のような回路が用いられている。

【0007】図6において、電源電圧Ｖｄｄと接地電圧Ｅ間に定電流源Ｉ６１とNチャンネル形のＭＯＳＦＥＴＱ６１とが直列に接続され、その接続点から出力電圧Ｖｏが出力される。また、差動増幅器ＣＰ６１が設けられ、その反転入力端子－に入力電圧Ｖｉｎが入力され、非反転入力端子＋に出力電圧Ｖｏが入力され、出力がＭＯＳＦＥＴＱ６１のゲートに印加される。

【0008】この図６の電源回路において、定電流源Ｉ６１から常時定電流ｉ１が供給される一方、入力電圧Ｖｉｎと出力電圧Ｖｏとが差動増幅器ＣＰ６１で比較され、その比較結果でＭＯＳＦＥＴＱ６１が導通制御されている。このため、出力電圧Ｖｏは入力電圧Ｖｉｎに等しくなるように制御されることになる。

【0009】ところで、液晶表示装置の駆動回路においては、容量性負荷を種々の電圧値のバイアス電圧を組み合わせて駆動することから、出力電圧Ｖｏが押し上げられたり、引き下げられたりする。いずれの原因にしても、出力電圧Ｖｏが所定の値から変動することになる。以後、この変動方向が正方向のものを正ノイズ（Ｈノイズ）、変動方向が負方向のものを負ノイズ（Ｌノイズ）とする。

【0010】さて、図６の電源回路では、Ｈノイズが発生し出力電圧Ｖｏが上昇すると、差動増幅器ＣＰ６１の出力電圧によりＭＯＳＦＥＴＱ６１が制御され、上昇した出力電圧Ｖｏを低下させ、出力電圧Ｖｏが入力電圧Ｖｉｎになった時点で動作が停止する。従って、その上昇した出力電圧Ｖｏを低下させる能力はＭＯＳＦＥＴＱ６１のドライブ能力に依って定まることになる。

【0011】一方、Ｌノイズが発生し出力電圧Ｖｏが低下すると、まず差動増幅器ＣＰ６１の出力電圧によりＭＯＳＦＥＴＱ６１が制御される。そして、定電流源Ｉ６１を通して定電流ｉ１が注入され、時間の経過につれて出力電圧Ｖｏが上昇していく。そして、出力電圧Ｖｏが入力電圧Ｖｉｎに等しくなったときに、差動増幅器ＣＰ６１の出力がハイレベルとなりＭＯＳＦＥＴＱ６１が導通して、常に出力電圧Ｖｏが入力電圧Ｖｉｎに等しくなるように制御される。従って、その低下した出力電圧Ｖｏを上昇させる能力は定電流源Ｉ６１のｉ１の大きさに依って定まることになる。

【0012】そして、この出力電圧Ｖｏを入力電圧Ｖｉｎに等しく保つために、ＭＯＳＦＥＴＱ６１は定電流源Ｉ６１のｉ１を定常的に流し続けることになる。

【0013】このように出力電圧のノイズ成分、特に負ノイズ成分を低くするためには、定電流源Ｉ６１のｉ１を大きくする必要があるが、このことは液晶表示装置における大きな目標である低消費電力化と相反する状態になる。

【0014】図7は、このような図６における問題を改善する従来の電源回路であり、図６における定電流源Ｉ６１に並列に、Ｐチャンネル形ＭＯＳＦＥＴＱ６２と定電流源Ｉ６２の直列回路を設けたものである。その他の構成、作用は図６におけると同様である。

【0015】図7で、出力電圧Ｖｏにノイズの乗りやすいタイミング時に定期的に、ＭＯＳＦＥＴＱ６２のゲー

トにオン制御信号を与えて、ＭＯＳＦＥＴＱ６２を導通させ、定電流源Ｉ６２の定電流ｉ２を定電流源Ｉ６１の定電流ｉ１に重畳させる。これにより、特にＬノイズ時の対応能力を高めようとするものである。

【００１６】しかし、ＭＯＳＦＥＴＱ６２の導通は、出力電圧Ｖｏへのノイズ成分の有無に関わらず、定期的に行われるものであるため、Ｌノイズ時の対応能力は多少は改善されるものの、基本的な解決手段とはなり得ないものであった。

【００１７】

【発明が解決しようとする課題】このように、従来の電源回路では、出力電圧のノイズ成分、特に負ノイズ成分を低くするためには、定電流源の電流値を大きくする必要があるが、このことは電源回路の低消費電力化と相反する状態になってしまうと言う問題があった。

【００１８】そこで、本発明は、ボルテージフォロワの出力段を構成する電源回路において、出力電圧へのノイズ成分の除去能力を向上し、容量性負荷の駆動能力を大きくすると共に、低消費電力化も合わせて達成できる電源回路を提供することを目的とする。

【００１９】

【課題を解決するための手段】請求項１の電源回路は、出力端子と第１電源Ｅ間に接続された第１スイッチング素子Ｑ１１と、第２電源Ｖｄｄと前記出力端子間に接続された第２スイッチング素子Ｑ１２と、入力電圧Ｖｉｎと前記出力端子の出力電圧Ｖｏとを比較し、この出力電圧Ｖｏが入力電圧Ｖｉｎを上回るときに、前記第１スイッチング素子Ｑ１１を導通させる第１比較器ＣＰ１１と、参照電圧Ｖｒｅｆと前記出力電圧Ｖｏとを比較し、この出力電圧Ｖｏが前記参照電圧Ｖｒｅｆを下回るときに、前記第２スイッチング素子Ｑ１２を導通させる第２比較器ＣＰ１２とを備え、該第２比較器ＣＰ１２の動作にヒステリシス特性を持たせたことを特徴とする。

【００２０】請求項１の電源回路によれば、出力電圧Ｖｏを上昇させる時に第２スイッチング素子Ｑ１２を導通させるから、従来の定電流型電源回路に比べて、負荷駆動能力が著しく向上する。

【００２１】また、第２スイッチング素子Ｑ１２を設け、且つこの第２スイッチング素子Ｑ１２の導通／非導通を制御する比較器ＣＰ１２にヒステリシス特性を持たせたことにより、ノイズ成分の除去能力を向上することができると共に、出力電圧における歪み成分を極めて小さくすることができる。

【００２２】また、第１スイッチング素子Ｑ１１と第２スイッチング素子Ｑ１２とをそれぞれ比較器ＣＰ１１，比較器ＣＰ１２で同時に導通することがないように制御することで、電源間の貫通電流が発生することはなく、併せて負荷が容量性負荷の場合には消費電力はほとんど無視できるから、低消費電力化が図られる。

【００２３】

【発明の実施の形態】以下、本発明の実施例について、図１～図４を参照して説明する。

【００２４】図１は、本発明の実施例に係る電源回路を示す図である。この図１において、電源電圧Ｖｄｄと接地電圧Ｅ間にＰチャンネル形のＭＯＳＦＥＴＱ１２とＮチャンネル形のＭＯＳＦＥＴＱ１１が直列に接続され、この接続点Ａから出力電圧Ｖｏが出力される。このＭＯＳＦＥＴＱ１２が負荷に給電するスイッチとして機能し、ＭＯＳＦＥＴＱ１１が吸収するためのスイッチとして機能する。そして、差動増幅器ＣＰ１１の反転入力端子－に入力電圧Ｖｉｎが入力され、非反転入力端子＋に出力電圧Ｖｏが入力され、比較器として機能し、その出力がＭＯＳＦＥＴＱ１１のゲートに印加される。

【００２５】また、差動増幅器ＣＰ１２の反転入力端子－には参照電圧Ｖｒｅｆ１あるいはＶｒｅｆ２が入力され、非反転入力端子＋には出力電圧Ｖｏが入力され、比較器として機能し、その出力（Ｃ点電位）がＭＯＳＦＥＴＱ１２のゲートに印加される。そして、電源電圧Ｖｄｄと接地電圧Ｅ間との間に抵抗Ｒ１１と抵抗Ｒ１２が直列接続され、抵抗Ｒ１３とＮチャンネル形ＭＯＳＦＥＴＱ１３の直列回路が抵抗Ｒ１２に並列接続されている。したがって、参照電圧であるＢ点電位は、ＭＯＳＦＥＴＱ１３の導通／非導通に応じて、参照電圧としてＶｒｅｆ１あるいはＶｒｅｆ２の２つの値のいずれかの値を取る。

【００２６】そして、このＭＯＳＦＥＴＱ１３のゲートには、Ｃ点電位、すなわち差動増幅器ＣＰ１２の出力電位が入力されるから、差動増幅器ＣＰ１２は出力電圧Ｖｏに関して、ヒステリシス特性を持つことになる。

【００２７】さて、この図１の電源回路の動作を、図２の特性図を参照しつつ説明する。まず、通常時の状態は、出力電圧Ｖｏは入力電圧Ｖｉｎとほぼ等しい電圧値にあり、ＭＯＳＦＥＴＱ１２はオフ状態、ＭＯＳＦＥＴＱ１１は不定（オンの場合もあるし、オフの場合もあり得る）の状態にある。差動増幅器ＣＰ１２の出力はＨレベルにあり、ＭＯＳＦＥＴＱ１３はオン状態で、Ｂ点電位は低い電位の参照電圧Ｖｒｅｆ２となっている。

【００２８】この電源回路の考え方を理解しやすくするために、これらの各電圧の関係を整理し、かつ仮定の具体的電位を設定すると、次のようになる。

Ｖｉｎ（３．０Ｖ）＝定常時のＶｏ＝Ｖｒｅｆ１＞Ｖｒｅｆ２（２．７Ｖ）

【００２９】この通常時の状態から、出力電圧ＶｏにＬノイズが重畳される（ｔ１）と、出力電圧Ｖｏは低下していき、そのときの参照電圧Ｖｒｅｆ２まで低下すると、差動増幅器ＣＰ１２の動作状態が反転し、その出力がＬレベルになる。したがって、ＭＯＳＦＥＴＱ１２がオフからオン状態になり、電源電圧Ｖｄｄから負荷に電流が供給され始める。また、この時、ＭＯＳＦＥＴＱ１３がオンからオフ状態になり、高い参照電圧Ｖｒｅｆ１

が差動増幅器ＣＰ１２に供給される。

【００３０】Ｌノイズのエネルギーが大きい場合には、出力電圧Ｖｏは参照電圧Ｖｒｅｆ２を越えてさらに低下し、時点ｔ２で上昇に転じる。この時、高い参照電圧Ｖｒｅｆ１となっているので、電源電圧ＶｄｄからＭＯＳＦＥＴＱ１２を介して電流が供給され続け、出力電圧Ｖｏが上昇を続ける。

【００３１】そして、出力電圧Ｖｏが高い参照電圧Ｖｒｅｆ１となった時点ｔ３で、差動増幅器ＣＰ１２の出力がＨレベルに反転し、ＭＯＳＦＥＴＱ１２がオフし、ＭＯＳＦＥＴＱ１３がオンし、低い参照電圧Ｖｒｅｆ２となり、通常の動作状態に復帰する。

【００３２】つまり、出力電圧Ｖｏに関して差動増幅器ＣＰ１２が、ヒステリシス動作を行っている。

【００３３】次に、通常時の動作状態から、出力電圧ＶｏにＨノイズが重畳される（ｔ４）と、出力電圧Ｖｏは上昇していく。この時、出力電圧Ｖｏが入力電圧Ｖｉｎを越えたときに、差動増幅器ＣＰ１１の出力はＨレベルとなるので、ＭＯＳＦＥＴＱ１１がオンしている。

【００３４】Ｈノイズのエネルギーにより、出力電圧Ｖｏは入力電圧Ｖｉｎより高い電圧まで上昇し、時点ｔ５で降下に転じる。その後、出力電圧Ｖｏは降下を続けて、入力電圧Ｖｉｎと等しくなった時点ｔ６で、ＭＯＳＦＥＴＱ１１がオフして、定常状態に回復する。

【００３５】本発明の実施例は、以上のように動作するが、この実施例の１つの特徴である差動増幅器ＣＰ１２のヒステリシスの作用について、理解を明確にするために、ヒステリシスを有さない参考例について、図３及び図４を用いて、説明する。

【００３６】この参考例は、図１，図２の本発明の実施例と比較して、参照電圧を高低の２値に切り替える点が無いだけで、その他は同じである。

【００３７】さて、この参考例において、出力電圧Ｖｏが入力電圧Ｖｉｎにある通常の動作状態から、出力電圧ＶｏにＬノイズが重畳される（ｔ１）と、出力電圧Ｖｏは低下していき、参照電圧Ｖｒｅｆまで低下すると、差動増幅器ＣＰ１２の動作状態が反転し、その出力がＬレベルになる。したがって、ＭＯＳＦＥＴＱ１２がオフからオン状態になり、電源電圧Ｖｄｄから負荷に電流が供給され始める。

【００３８】Ｌノイズのエネルギーにより、出力電圧Ｖｏは参照電圧Ｖｒｅｆを越えてさらに低下し、時点ｔ２で上昇に転じる。

【００３９】そして、出力電圧Ｖｏが参照電圧となった時点ｔ３で、差動増幅器ＣＰ１２の出力がＨレベルに反転し、ＭＯＳＦＥＴＱ１２がオフする。従って、出力電圧Ｖｏは定常動作状態より低い電圧Ｖｒｅｆに留まった状態となる。

【００４０】次に、この出力電圧Ｖｏが定常動作状態より低い電圧Ｖｒｅｆに留まった状態から、出力電圧ＶｏにＨノイズが重畳される（ｔ４）と、出力電圧Ｖｏは上昇していく。そして、出力電圧Ｖｏが入力電圧Ｖｉｎを越えたときに、差動増幅器ＣＰ１１の出力がＨレベルとなるので、ＭＯＳＦＥＴＱ１１がオンする。

【００４１】Ｈノイズのエネルギーにより、出力電圧Ｖｏは入力電圧Ｖｉｎより高い電圧まで上昇し、時点ｔ５で降下に転じる。その後、出力電圧Ｖｏは降下を続けて、入力電圧Ｖｉｎと等しくなった時点ｔ６で、ＭＯＳＦＥＴＱ１１がオフして、定常状態に回復する。

【００４２】このように、差動増幅器ＣＰ１２の動作にヒステリシスを持たない参考例では、一旦Ｌノイズに見舞われると、出力電圧Ｖｏは参照電圧Ｖｒｅｆまでしか回復できない。図４の説明のようにＨノイズがいつも到来してくれる訳ではなく、ヒステリシスを持たない場合には、どうしてもＬノイズに依る歪み分（Ｖｉｎ－Ｖｒｅｆ）が残ってしまうことになる。

【００４３】この場合、参照電圧Ｖｒｅｆを入力電圧Ｖｉｎに等しくする、あるいは近づけることが考えられるかも知れないが、電圧の設定誤差や、構成素子の特性のばらつきなどのために、安定した動作を確保することが難しく、ＭＯＳＦＥＴＱ１１とＭＯＳＦＥＴＱ１２とが同時に導通し、いわゆる貫通電流が電源間に流れることにもなる。このようなことを避けるために、参照電圧Ｖｒｅｆを入力電圧Ｖｉｎより少し低い値に設定せざるを得ないことになる。

【００４４】本発明実施例の電源回路によれば、負荷に給電したり、低下した出力電圧Ｖｏを上昇させる時にのみＭＯＳＦＥＴＱ１２をオン状態にするからそのインピーダンスを極めて小さくすることができる。このため、従来の定電流回路を用いた給電経路に比べて大きな電流を流すことができるから、高容量性負荷等の負荷駆動能力を高めることができる。

【００４５】また、この給電側のＭＯＳＦＥＴＱ１２のオン・オフを制御する差動増幅器ＣＰ１２にヒステリシス特性を持たせているから、Ｈノイズ成分あるいはＬノイズ成分のどちらのノイズに対しても、その除去能力を向上することができる。そして、出力電圧Ｖｏを正負いずれの方向からでも所定の電圧（Ｖｉｎ）にセットすることができるので、出力電圧Ｖｏにおける歪み成分を極めて小さくできる。

【００４６】また、給電側のＭＯＳＦＥＴＱ１２と吸収側のＭＯＳＦＥＴＱ１１とをそれぞれ差動増幅器ＣＰ１１，差動増幅器ＣＰ１２で同時に導通することがないように制御することで、電源間の貫通電流が発生することはない。また、併せて負荷が容量性負荷の場合には消費電力はほとんど無視できる。したがって、電源回路の低消費電力化が図られるし、回路装置のレイアウト寸法も小さくすることができる。

【００４７】

【発明の効果】本発明の電源回路によれば、出力電圧Ｖ

ｏを上昇させる時に第２スイッチング素子を導通させるから、従来の定電流型電源回路に比べて、負荷駆動能力が著しく向上する。

【００４８】また、第２スイッチング素子の導通／非導通を制御する比較器にヒステリシス特性を持たせたことにより、ノイズ成分の除去能力を向上することができると共に、出力電圧における歪み成分を極めて小さくすることができる。

【００４９】また、第１スイッチング素子と第２スイッチング素子とをそれぞれ比較器で同時に導通することがないように制御することで、電源間の貫通電流が発生することはなく、併せて負荷が容量性負荷の場合には消費電力はほとんど無視できるから、低消費電力化が図られる。

【図面の簡単な説明】

【図１】本発明の実施例に係る電源回路を示す図。

【図２】本発明の実施例に係る電源回路の動作を説明する図。

【図３】本発明の参考例に係る電源回路を示す図。

【図４】本発明の参考例に係る電源回路の動作を説明する図。

【図５】一般的な液晶表示装置を示す図。

【図６】従来の電源回路を示す図。

【図７】従来の電源回路を示す図。

【符号の説明】

Ｑ１１、Ｑ１３　Ｎチャンネル形ＭＯＳＦＥＴ

Ｑ１２　Ｐチャンネル形ＭＯＳＦＥＴ

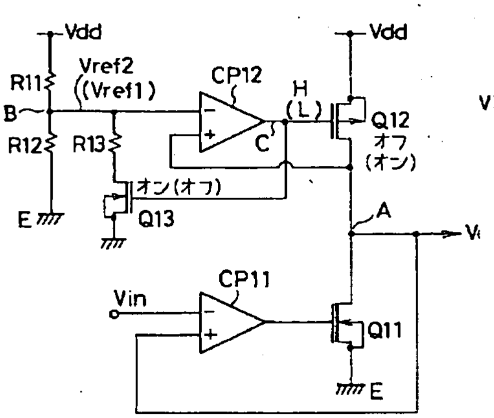
ＣＰ１１、ＣＰ１２　差動増幅器

Ｖｏ　出力電圧

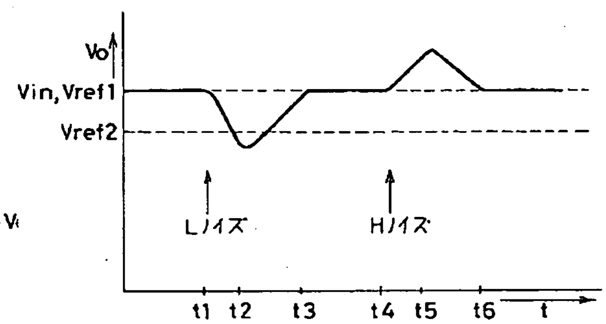
Ｖｉｎ　入力電圧

Ｖｒｅｆ１，Ｖｒｅｆ２　参照電圧

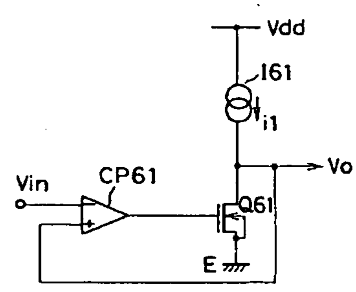
【図１】



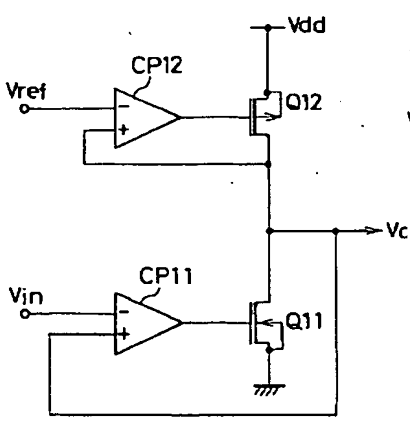
【図２】



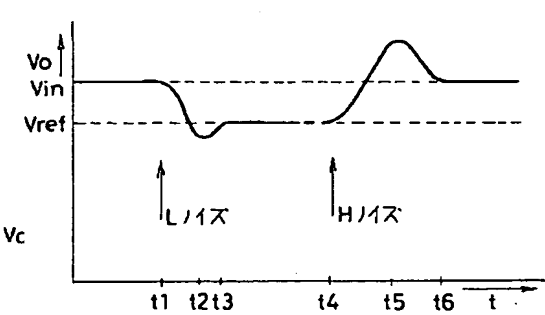
【図６】



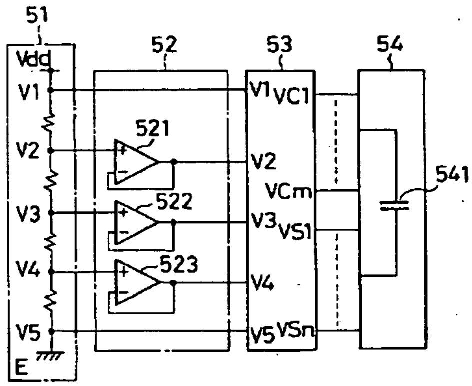
【図３】



【図４】

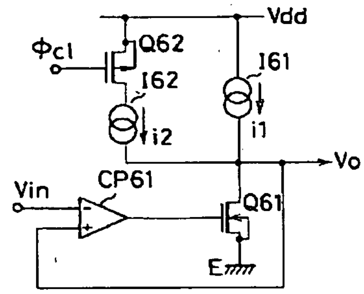


【図5】



51
52
53
54
Vdd
V1
V2
V3
V4
V5
E
521
522
523
V1
VC1
V2
VCm
V3
VS1
V4
V5
VSn
541

【図7】



Vdd
Φc1
Q62
I62
I61
i2
i1
Vo
Vin
CP61
Q61
E

US006426670B1

(12) United States Patent
Tanaka

(10) Patent No.: US 6,426,670 B1
(45) Date of Patent: Jul. 30, 2002

(54) POWER CIRCUIT WITH COMPARATORS AND HYSTERESIS

(75) Inventor: Toshimasa Tanaka, Kyoto (JP)

(73) Assignee: Rohm Co., Ltd., Kyoto (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/650,295

(22) Filed: Aug. 29, 2000

(30) Foreign Application Priority Data

Aug. 30, 1999 (JP) 11-242509

(51) Int. Cl.[7] G05F 1/46

(52) U.S. Cl. 327/541; 327/543; 323/274; 323/275; 323/280; 323/281; 345/211

(58) Field of Search 327/112, 538, 327/540, 541, 543; 323/311, 313, 274, 275, 280, 281, 283, 284; 345/98, 99, 211, 212

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Primary Examiner—Timothy P. Callahan
Assistant Examiner—Terry L. Englund
(74) *Attorney, Agent, or Firm*—Hogan & Hartson, L.L.P.

(57) ABSTRACT

A power circuit having an output stage which includes voltage followers. The power circuit comprises first and second switching elements, respectively, connected between two voltage sources. A first comparator is provided to compare an input voltage with the output voltage of a voltage follower associated with the input voltage, and turn on the first switching element if the output voltage exceeds the input voltage. In addition, a second comparator is provided to compare the output voltage with a reference voltage to turn on the second switching element if the output voltage becomes lower than the reference voltage. A reference voltage circuit changes the value of the reference voltage depending on the output of the second comparator.

20 Claims, 6 Drawing Sheets

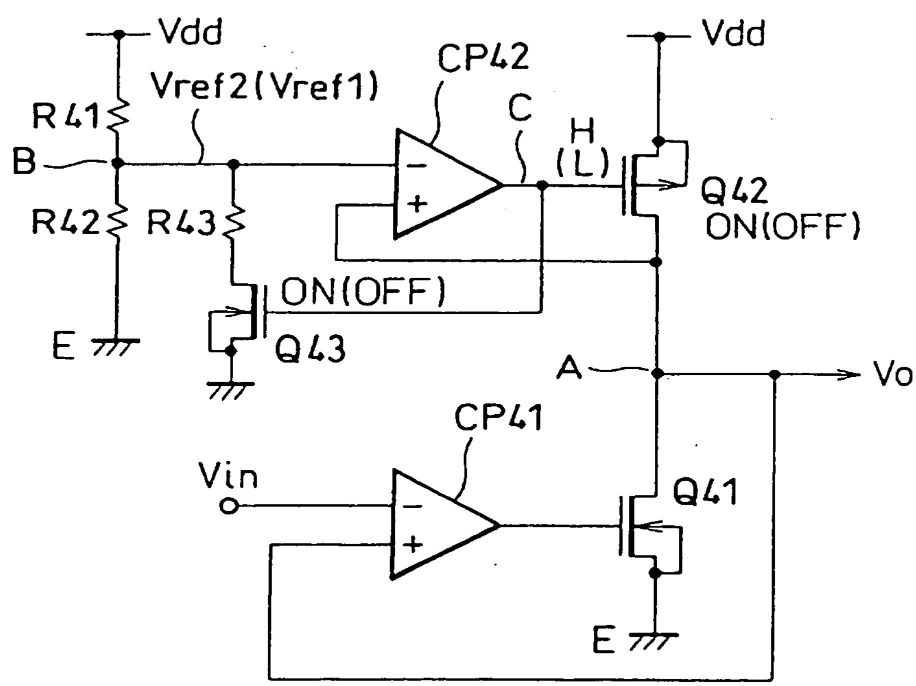


FIG.1
PRIOR ART

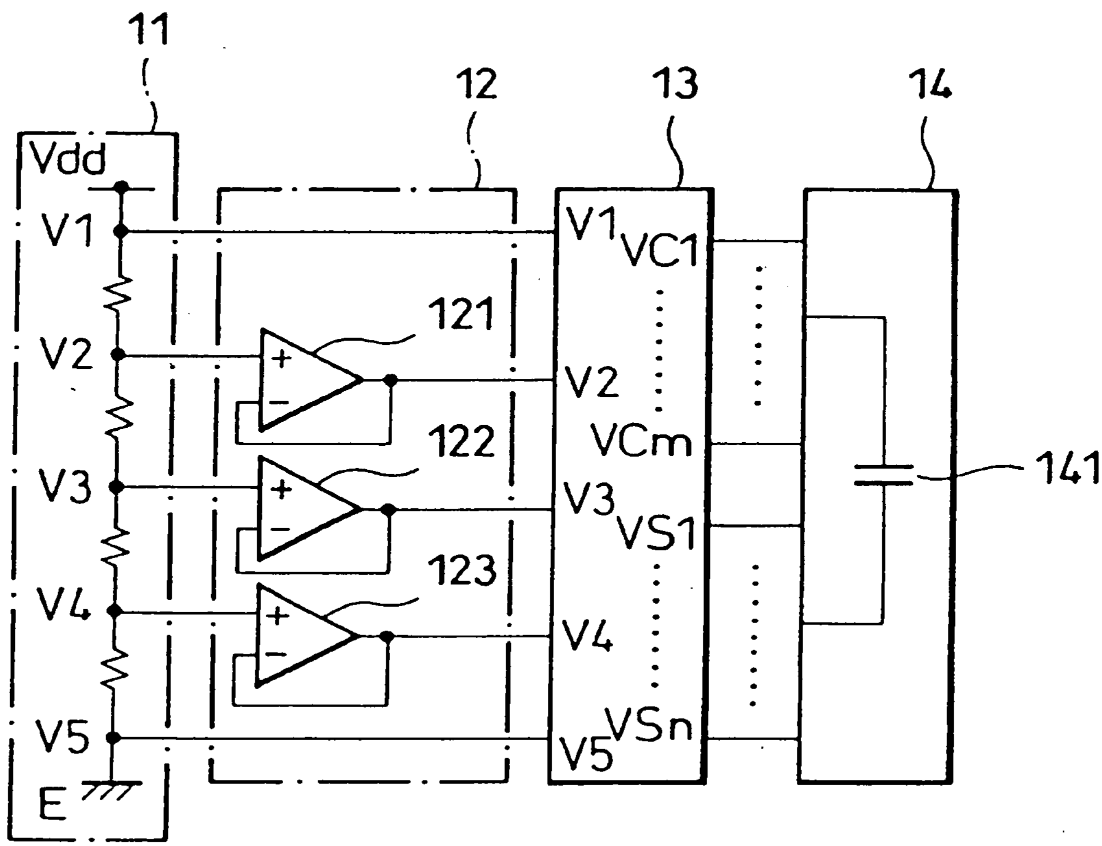


FIG. 2
PRIOR ART

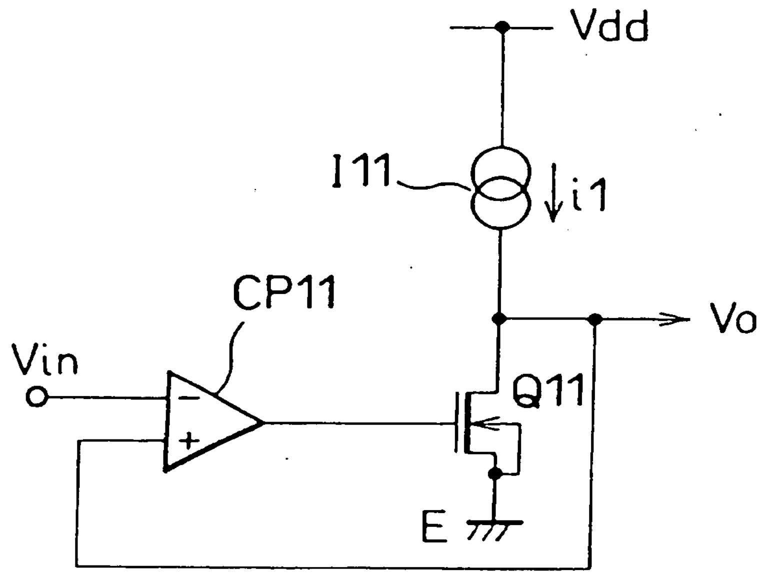


FIG. 3
PRIOR ART

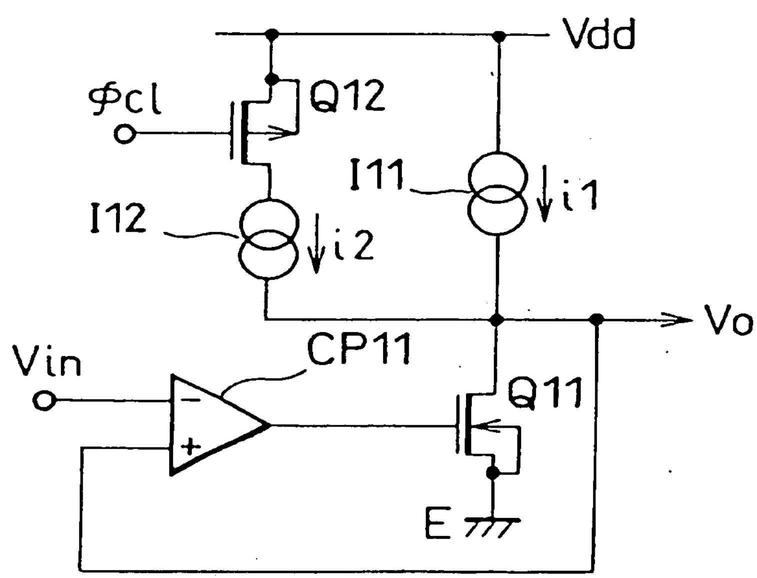
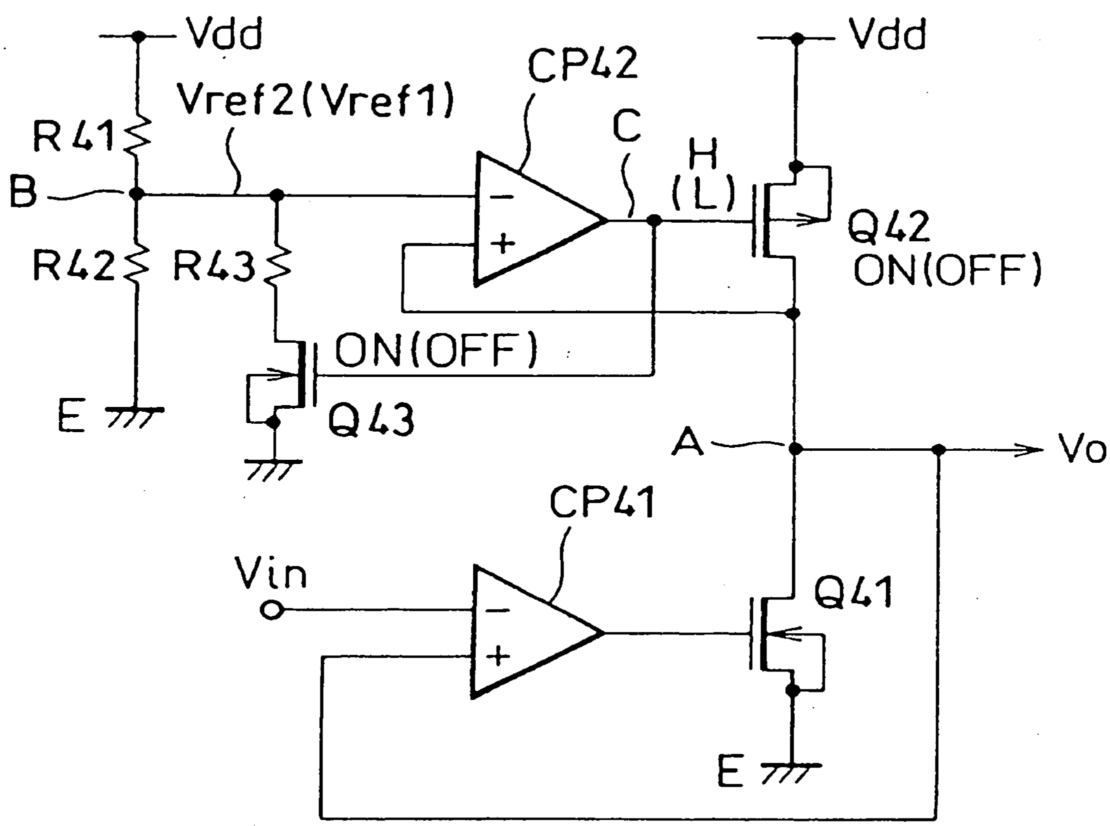


FIG.4



Vdd
R41
Vref2(Vref1)
CP42
C
H
(L)
Vdd
B
Q42
ON(OFF)
R42
R43
ON(OFF)
E
Q43
A
Vo
CP41
Vin
Q41
E

FIG. 5

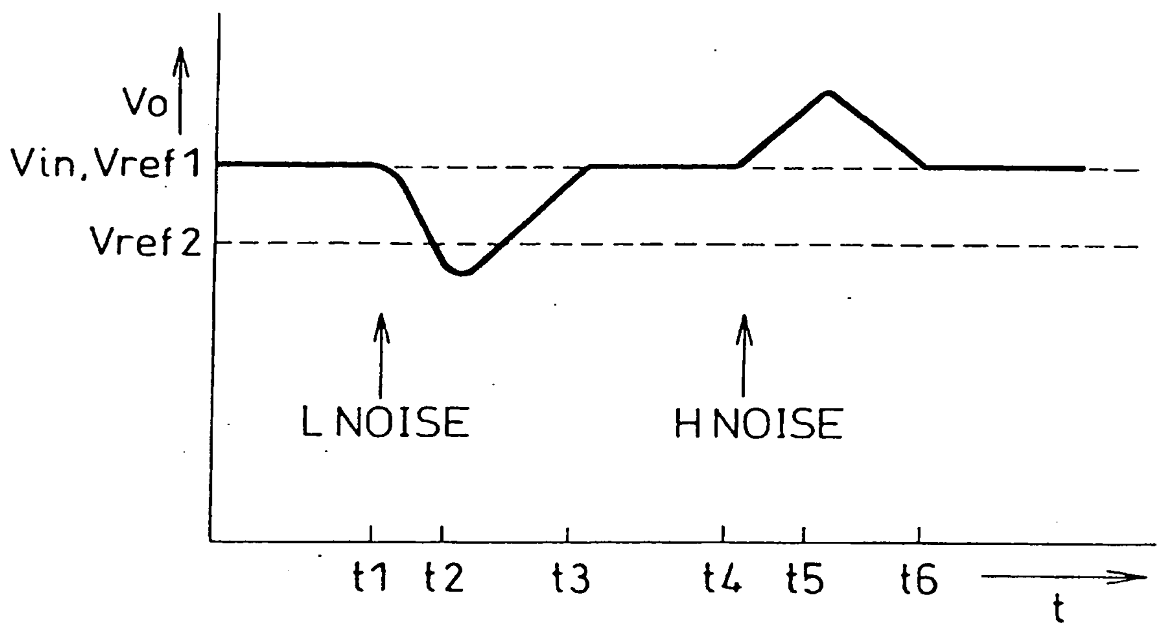


FIG. 6

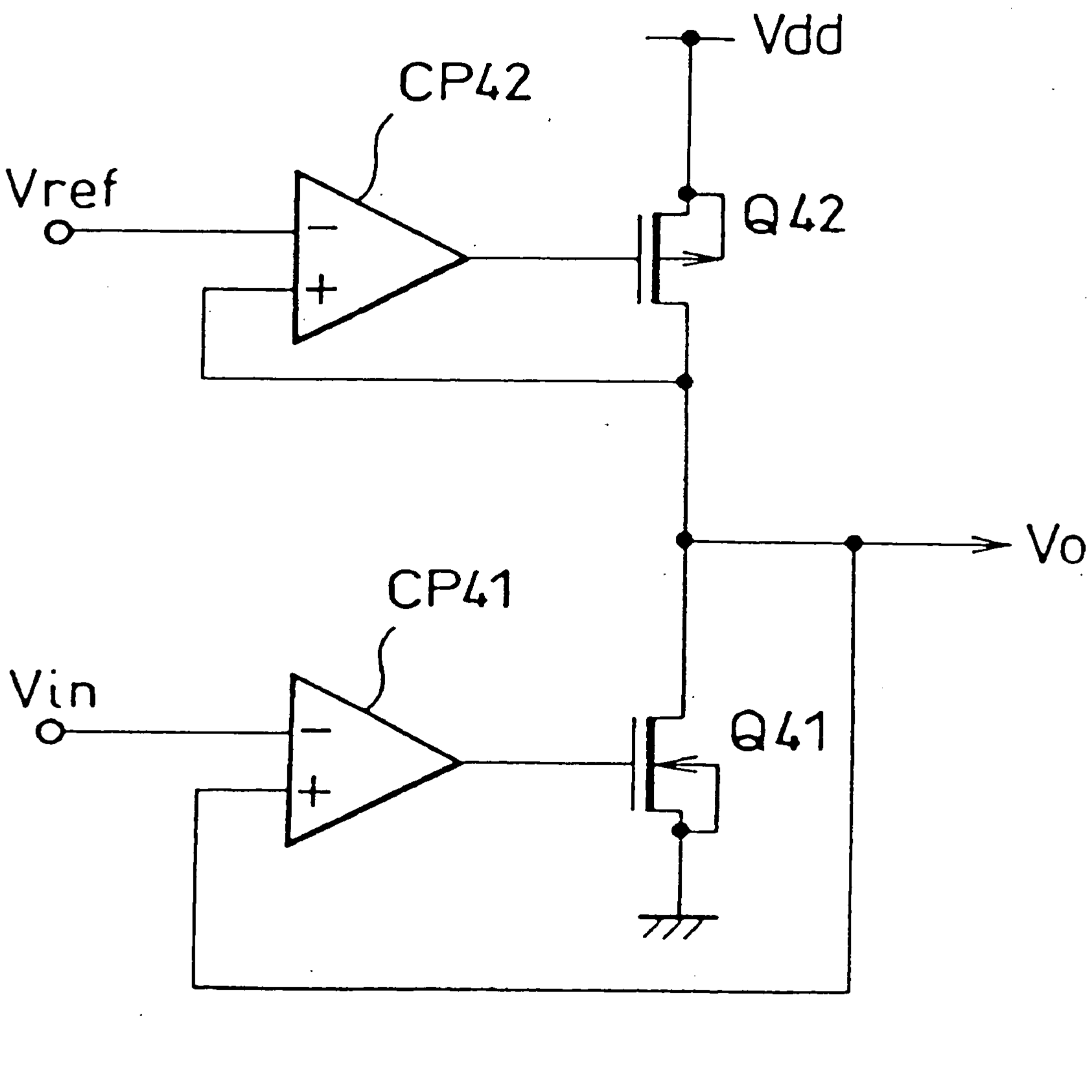
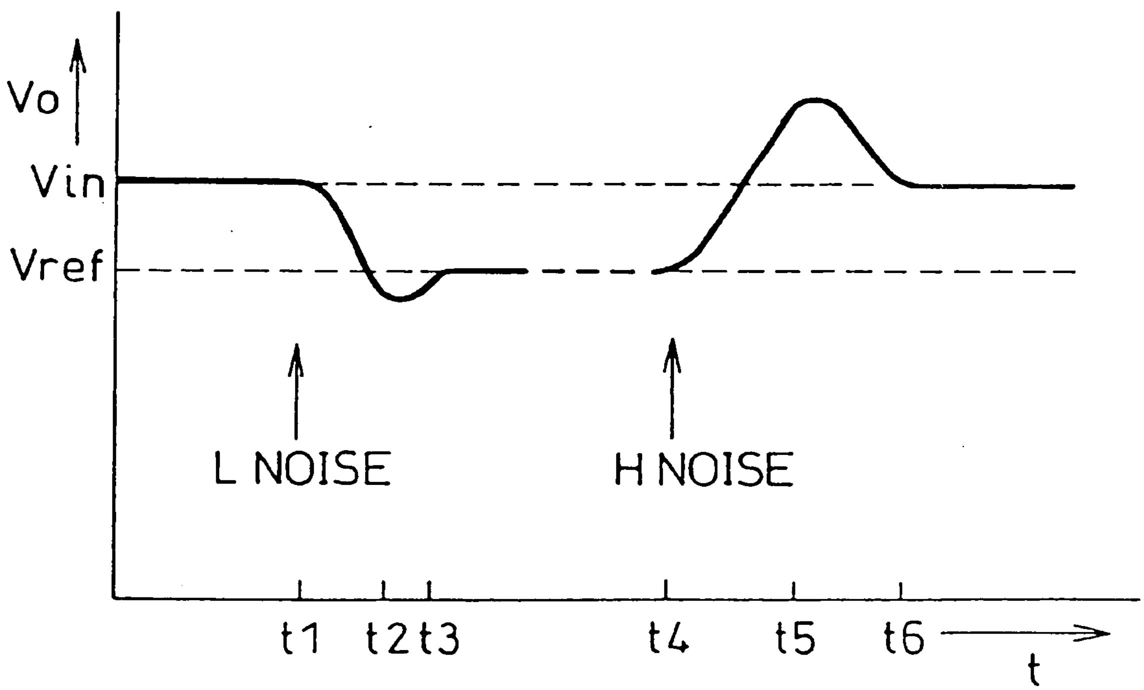


FIG. 7



POWER CIRCUIT WITH COMPARATORS AND HYSTERESIS

FIELD OF THE INVENTION

The invention relates to a power circuit for performing impedance conversion of a given voltage to provide an output, in particular to a power circuit for use in a liquid crystal display (LCD) apparatus which requires a multiplicity of voltage sources.

BACKGROUND OF THE INVENTION

Apparatuses have been commonly used as display means for portable communication devices such as cellular phones and pagers. In an LCD apparatus, a drive circuit is used to drive a multiplicity of display elements or pixels in a given duty cycle using a multiplicity of bias voltages as shown in FIG. 1.

The LCD apparatus of FIG. 1 comprises:

- a bias circuit **11** for generating a multiplicity of bias voltages by dividing a voltage between a source voltage Vdd and a ground voltage E by a multiplicity of series resistors each having a resistance of about 1 M Ohms;
- a buffer circuit **12** having voltage followers **121–123** for generating outputs by impedance conversion of the respective bias voltages;
- a selection circuit **13** for selectively applying the output voltages of the buffer circuit **12** to the display elements **141** of the LCD to be activated in accordance with the display data; and
- a display panel **14** on which a display pattern associated with the display data is formed by the pixels **141** thus activated.

In the duty operation by the multiplicity of bias voltages, those pixels having voltages applied to the electrodes thereof in excess of a predetermined level will be turned on.

An LCD apparatus having such arrangement must be operated at a low power on the one hand in order to maximize the life of the LCD as much as possible, but on the other hand, in order to provide a good display quality, it must be operable by a large driving power to prevent deterioration of output waveforms especially for a large capacitive load.

To meet these conflicting requirements, conventional LCD apparatuses employ a power circuit formed of voltage followers in a buffer circuit as shown in FIGS. 2 and 3.

As shown in FIG. 2, connected between the source voltage Vdd and the ground voltage E are a constant current source I11 and an N channel MOSFET Q11 connected in series with each other, providing at the node therebetween an output voltage Vo. A difference amplifier CP11 is also provided in the power circuit, having a negative or inverting input terminal for receiving an input voltage Vin and a positive or non-inverting input terminal for receiving the output voltage Vo, and generating a gate voltage for the MOSFET Q11.

In the power circuit shown in FIG. 2, a constant current i1 is provided from the constant current source I11. The input voltage Vin and the output voltage Vo are compared in the difference amplifier CP11 to control switching operation of the MOSFET Q11. The output voltage Vo is controlled to balance the input voltage Vin.

In an LCD apparatus capacitive loads are driven by combinatory voltages formed of different bias voltages, which cause such output voltage Vo to fluctuate up and down. Thus, the output voltage Vo deviates off a predetermined voltage for unspecified noise sources. In what follows a noise that causes an upward shift of the output voltage Vo will be referred to as positive noise or H noise, and a noise that causes a downward shift of the output voltage Vo will be referred to as negative noise or L noise.

In the power circuit shown in FIG. 2, as the output voltage Vo is pushed up appreciably by an H noise, the MOSFET Q11 is turned on by the output voltage of the difference amplifier CP11 to lower the output voltage Vo, until the output voltage Vo balances the input voltage Vin. Thus, the ability of the circuit to lower the output voltage Vo raised by a positive noise depends on the driving power of the MOSFET Q11.

On the other hand, if the output voltage Vo is lowered by an L noise, the MOSFET Q11 is turned off by the output of the difference amplifier CP11, and a s a result, a constant current i1 is supplied from the constant current source I11, which gradually pushes up the output voltage Vo. The output level of the difference amplifier CP11 will become high to turn the MOSFET Q11 as t he output voltage Vo equals the input voltage Vin, thereby keeping the output voltage Vo at the same level of the input level Vin. Thus, the ability of the power circuit to raise lowered output voltage Vo is determined by th e magnitude of the constant current i1 from the constant current source I11.

It is noted that the MOSFET Q11 keeps the current i1 flowing to have the output voltage Vo balancing the input voltage Vin.

In this way, in order to suppress noises, especially L noises, it is necessary to make the constant current i1 sufficiently large, which opposes, however, the aforementioned requirement that the power to drive the LCD circuit should be low.

FIG. 3 illustrates a conventional circuit with an improvement to overcome such problem as discussed above in conjunction with FIG. 2, in which a P channel MOSFET Q12 and a further constant current source I12 are connected in parallel with the constant current source I11. The basic structure and function of the improved circuit are the same as those of FIG. 2.

In the arrangement shown in FIG. 3, the MOSFET Q12 is supplied at the gate thereof with a periodic control signal for turning on the MOSFET Q12 at times when noises are supposedly likely to superpose on the output voltage Vo, thereby turning on the MOSFET Q12 to provide an extra constant current i2 from the constant current source I12 superposing on the constant current i1 from the constant current source I11, which adds to the power circuit a counteractive power against L-noises.

However, in this arrangement, the MOSFET Q12 is turned on periodically, irrespective of whether a noise exists affecting the output voltage Vo or not. Hence, although anti-L noise capacity is improved a little, the improvement cannot be a fundamental solution to the drive circuit for LCD apparatus.

"We see therefore that conventional drive circuits still suffer from a contradiction in suppressing the constant current on the one hand to prolonging the life of an LCD apparatus, and enhancing the current to suppress noises, especially L noises."

SUMMARY OF THE INVENTION

In accordance with one aspect of the invention, there is provided a power circuit comprising:

- a first switching element connected between an output terminal of the power circuit and a first voltage supply;
- a second switching element connected between a second voltage supply and the output terminal;

a first comparator for comparing an input voltage with an output voltage at the output terminal, to turn on the first switching element if the output voltage exceeds the input voltage;

a second comparator, having an input end and an output end, for comparing the output voltage with a reference voltage, to turn on the second switching element if the output voltage becomes lower than the reference voltage; and a reference voltage circuit for changing the reference voltage depending on a voltage value at the output end.

The second switching element of the power circuit is turned on in raising the output voltage, so that the power need to run a load is significantly reduced as compared with conventional constant current type power circuits.

The second comparator exhibits hysteresis during operation. The hysteresis of the second comparator controlling the second switching element may improve noise reduction, and hence output distortions caused by the noise in the power circuit.

By controlling the first and second comparators, respectively, so as not to make the first and the second switching elements conductive simultaneously, no inter-power supply current will be generated in the power circuit. Thus, power consumption by the power circuit of the invention is greatly reduced.

The reference voltage circuit may include a resistor and a third switching element controlled by the voltage value at the output end and provided between the input end of the second comparator for receiving the reference voltage and either one of the first voltage supply and the second voltage supply.

In this arrangement, the reference voltage to the second comparator is automatically switched between two levels in accordance with the output of the second comparator. In other words, the arrangement adds to the second comparator a hysteresis character with respect to the output voltage.

The third switching element as well as the first and the second switching elements, respectively, can be MOSFETs.

Further, the first switching element can be an N channel MOSFET, the second switching element can be a P channel MOSFET, and the third switching element can be an N channel MOSFET.

The power circuit having this arrangement can control the switching elements involved at a very low power in response to the output voltages of the first and second comparators, respectively.

In accordance with another aspect of the invention, there is provided a display apparatus comprising a bias circuit, a buffer circuit electrically coupled to the bias circuit, a selection circuit electrically coupled to the buffer circuit, and a display panel electrically coupled to the selection circuit, wherein the buffer circuit is made up of the previously mentioned power circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a typical LCD apparatus.;

FIG. 2 is a conventional power circuit for use in an LCD as shown in FIG. 1;

FIG. 3 is a similar conventional power circuit;

FIG. 4 is a circuit diagram of a power circuit according to the invention;

FIG. 5 is a graph illustrating a behavior of the power circuit of FIG. 4;

FIG. 6 is a circuit useful in understanding the power circuit of FIG. 4 of the invention;

FIG. 7 is a graph illustrating a behavior of the circuit of FIG. 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIGS. 4 though 7, the invention will now be described in detail. Referring first to FIG. 4, there is shown an exemplary power circuit according to the invention for use as voltage followers for example.

As shown in FIG. 4, a P channel MOSFET Q42 and an N channel MOSFET Q41 are connected in series between a first voltage supply providing a supply voltage Vdd and a second voltage supply E providing the ground voltage, to generate at the node A thereof an output voltage Vo. The MOSFET Q42 serves as a switch for supplying electric power to a capacitive load such as a common electrode of an LCD selectively connected to the node A, while the MOSFET Q41 serves as a switch for draining electric energy from the load.

When an input voltage Vin is entered at an inverting terminal of a difference amplifier CP41, and the output voltage Vo is entered at a non-inverting input terminal of the difference amplifier CP41, the difference amplifier CP41 serves as a comparator comparing the two inputs to generate an output, which is supplied to the gate of the MOSFET Q41.

The inverting input terminal of the difference amplifier CP42 is supplied with a reference voltage Vref which selectively assumes either a high reference voltage Vref1 or a low reference voltage Vref2 in accordance with the condition of the power circuit. The output voltage Vo is input to the non-inverted input terminal of the difference amplifier CP42 serving as a comparator. The output voltage Vo is compared with the reference voltage. The output of the comparator (potential at point C) is applied to the gate of the MOSFET Q42. Connected between the voltage supply at voltage Vdd and the ground at voltage E are resistors R41 and R42 connected in series. A resistor R43 and an N channel MOSFET Q43 connected in series with each other are connected in parallel with the resistor R42.

Consequently, point B has a reference voltage which equals either Vdd×R42/(R41+R42) (referred to as the high reference voltage Vref1) or Vdd×(R42×R43)/(R41×R42+R42×R43+R43×R41) (referred to as lower reference voltage Vref2), depending on whether the MOSFET Q43 is turned on or off.

The gate of the MOSFET Q43 is connected to the output of the difference amplifier CP42, so that the gate has the same voltage as the output. Hence the difference amplifier CP42 exhibits a hysteresis.

In most cases, the high reference voltage Vref1 is the same as the input voltage Vin. Any one of the outputs of the bias circuit 11 of LCD apparatus shown in FIG. 1 can be used as the input voltage Vin.

Referring to FIG. 5, the operation of the power circuit shown in FIG. 4 will now be described. This power circuit may be used as a drive circuit of an LCD apparatus in driving capacitive loads, where various bias voltages are generated and used in combination. The power circuit shown in FIG. 4 may provide such bias voltage, thus, under the influences of these bias voltages, the output voltage Vo deviates from a predetermined level because it is pushed up by H noises or pulled down by L noises.

Under a normal operating condition, the output voltage Vo is substantially the same as the input voltage Vin, and the MOSFET Q42 is turned off. The condition of the MOSFET Q41 is indefinite in that it can assume the ON state and the OFF state equally well. Meanwhile, the output of the difference amplifier CP42 is at H level and the MOSFET Q43 is in the ON state, so that the B point voltage equals the lower reference voltage Vref2.

To help readers understand the operation of the power circuit, relationships among various voltages involved is shown below, using tentative voltages.

$$Vin\ (3.0\ \mathrm{V}) = Vo\ \text{(under normal operation)}$$
$$= Vref1 > Vref2\ (2.7\ \mathrm{V})$$

If an L noise is superposed on the output voltage Vo (at time t1), the output voltage Vo tends to decrease. As the output voltage Vo is lowered to the level of the reference voltage Vref2, the output of the difference amplifier CP42 is inverted, generating at the output terminal thereof a low level voltage L. Consequently, the MOSFET Q42 is turned ON, resulting in a current flowing from the voltage supply at Vdd through the MOSFET Q42. At the same time, the MOSFET Q43 is turned OFF, providing the difference amplifier CP42 with the high reference voltage Vref1.

If, however, the output voltage Vo is lower than the normal operating voltage, i.e. Vin, the MOSFET Q41 is turned OFF since then the output voltage of the MOSFET Q41 is low L.

Upon activation of the MOSFET Q42, a current is supplied from the voltage supply Vdd to the load. If a large L noise exists, the output voltage Vo will become lower than the reference voltage Vref2 (at time t1) and will begin to increase some time later at time t2. In this case, since the reference voltage of the difference amplifier CP42 is high Vref1, the current keeps flowing from the supply voltage Vdd through the MOSFET Q42 which causes the output voltage Vo to rise above the low reference voltage Vref2.

As the output voltage Vo reaches the high reference voltage Vref1 at time t3, the output of the difference amplifier CP42 is inverted to high level H. This turns the MOSFET Q42 off and the MOSFET Q43 on, so that the reference voltage Vref for the difference amplifier CP42 becomes low Vref2, thereby allowing the power circuit to restore the normal operating condition.

In short, in the power circuit shown in FIG. 4, the difference amplifier CP42 has hysteresis with respect to the output voltage Vo.

If, on the other hand, an H noise is superposed on the output voltage Vo during a normal operation, at time t4 say, the output voltage Vo rises. It continues to increase until it exceeds the input voltage Vin, when the output of the difference amplifier CP41 becomes high H to turn on the MOSFET Q41.

While the output voltage Vo is above the normal level, the output of the difference amplifier CP42 is high H and the MOSFET Q42 is turned off.

As the MOSFET Q41 is turned on, a current is drawn from the load. Meanwhile, the output voltage Vo increases above the input voltage Vin due to the energy of the H noise, and begins to decrease later at time t5. The output voltage Vo will further decrease, until it balances the input voltage Vin at t6 say to turn off the MOSFET Q41, allowing the power circuit to return to the normal operating condition.

It is seen that the power circuit of the invention advantageously operates as describe above, owing to the hysteresis character of the difference amplifier CP42. This feature of the invention will be better understood by comparing the invention with a referential circuit as shown in FIG. 6, having no hysteresis character. The behavior of the circuit of FIG. 6 is shown in FIG. 7.

The referential circuit shown in FIG. 6 has the same structure as the inventive circuit shown in FIGS. 4 and 5 except that the former circuit has only one reference voltage Vref.

In the referential circuit shown herein the reference voltage Vref is set a little lower than that of the input voltage Vin. Since the driving power of the MOSFET Q42 is made as large as that of the MOSFET Q41 to enable quick absorption of noise from the load, this lower setting of the reference voltage is necessary because otherwise the MOSFET Q41 and the MOSFET Q42 would be simultaneously conducted, resulting in a large current between the voltage supply at Vdd and the ground.

Under a normal operating condition where the output voltage Vo is held at the input voltage Vin, if an L noise is superposed on the output noise Vo (at time t1), the output voltage Vo decreases with time as low as the reference voltage Vref, at which the difference amplifier CP42 is inverted and its output shifts to a low level L. Thus, the MOSFET Q42 is turned on, causing the voltage supply Vdd to supply a current to the load.

On account of the energy brought by the L noise, the output voltage Vo is further lowered below the reference voltage Vref, until the energy is exhausted at time t2 when the output voltage Vo begins to rise.

When the output voltage Vo balances the reference voltage Vref at time t3, the output of the difference amplifier CP42 is inverted from L to H, so that the MOSFET Q42 is turned off. Consequently, the output voltage Vo remains at the level of the reference voltage Vref which is lower than the anticipated normal output voltage.

If then an H noise is superposed on the output voltage Vo (at time t4) while the output voltage Vo is at Vref, the output voltage Vo begins to rise. As the output voltage Vo exceeds the input voltage Vin, the difference amplifier CP41 is turned on by the high output (H) of the difference amplifier CP41.

The output voltage Vo overshoots the input voltage Vin due to the energy of the H noise at t5, and thereafter begins to decrease as shown in FIG. 7. The output voltage Vo continues to decrease until it balances the input voltage Vin at time t6, when the MOSFET Q41 is turned off to restore the normal operating condition of the power circuit.

In this way, once disturbed by an L noise, the power circuit can recover the output voltage only up to the reference voltage Vref if the difference amplifier CP42 has no hysteresis character. Therefore, the distortion in the output of the power circuit caused by an L noise remains as much as (Vin−Vref), unless an H noise follows the L noise as shown in FIG. 7. However, one may not always anticipate such H noise to restore the output.

As a solution to eliminate such L noise distortion, the reference voltage Vref could be set equal to or close to the input voltage Vin. However, since there is always some error involved in setting the reference voltage and there is always some allowance in the rating of the components used, it is difficult to set up an exact reference voltage Vref as desired, and therefore there is always a chance of simultaneous conduction of the MOSFET Q41 and MOSFET Q42, which results in a so-called inter-power supply current between the

power supplies. In order to avoid such drawbacks, it is inevitable to set the reference voltage Vref a little lower than the input voltage Vin.

In contrast, the invention allows the MOSFET Q42 to be turned on only when a current is required for the load or for raising the lowered output voltage Vo to the normal level, as described in conjunction with FIGS. 4 and 5. This implies that the impedance of the MOSFET Q42 can be very small. Thus, the power circuit of the invention can provide a much greater current to the load as compared with conventional constant current type power circuits, which implies that the power circuit of the invention has an enhanced driving power to a highly capacitive load.

It will be recalled that because of the hysteresis character of the difference amplifier CP42 controlling ON/OFF operations of the MOSFET Q42, the power circuit of the invention can minimize the influences of both H noises and L noises. It should be appreciated that the output voltage Vo can be set to a given input voltage Vin from above and below Vin, corrected to the level of the input voltage Vin if the output voltage is deviated above or below Vin.

It will be also recalled that the current providing MOSFET Q42 and the current absorbing MOSFET Q41 are conditioned not to be conductive simultaneously by the respective difference amplifiers CP41 and CP42, so that an inter-source current will never be incurred. In addition, the power consumption by the power circuit will be negligibly small if the load is capacitive. Thus, the invention enables a design of a compact power circuit which includes advantageously smaller elements such as MOSFETs consuming only a small amount of electric energy.

What I claim is:

1. A power circuit comprising:

a first switching element connected between an output terminal of the power circuit and a first voltage supply;

a second switching element connected between a second voltage supply and said output terminal;

a first comparator for comparing an input voltage with an output voltage at said output terminal, to turn on said first switching element if said output voltage exceeds said input voltage;

a second comparator, having an input end and an output end, for comparing said output voltage with a reference voltage, to turn on said second switching element if said output voltage becomes lower than said reference voltage; and

a reference voltage circuit for changing said reference voltage depending on a voltage value at said output end.

2. The power circuit as set forth in claim 1, wherein said reference voltage circuit includes a resistor and a third switching element controlled by said voltage value at said output end and provided between said input end of said second comparator for receiving said reference voltage and either one of said first voltage supply and said second voltage supply.

3. The power circuit as set forth in claim 2, wherein said first, second and third switching elements are MOSFETs.

4. The power circuit as set forth in claim 3, wherein said first switching element is an N channel MOSFET and said second switching element is a P channel MOSFET.

5. The power circuit as set forth in claim 3, wherein said third switching element is an N channel MOSFET.

6. The power circuit as set forth in claim 1, wherein said second comparator exhibits hysteresis during operation.

7. A display apparatus comprising:

a bias circuit;

a buffer circuit electrically coupled to said bias circuit comprising;

a first switching element connected between an output terminal of said buffer circuit and a first voltage supply;

a second switching element connected between a second voltage supply and said output terminal;

a first comparator for comparing an input voltage with an output voltage at said output terminal, to turn on said first switching element if said output voltage exceeds said input voltage;

a second comparator, having an input end and an output end, for comparing said output voltage with a reference voltage, to turn on said second switching element if said output voltage becomes lower than said reference voltage; and

a reference voltage circuit for changing said reference voltage depending on a voltage value at said output end; and

a selection circuit electrically coupled to said buffer circuit; and

a display panel electrically coupled to said selection circuit.

8. The display apparatus as set forth in claim 7, wherein said reference voltage circuit includes a resistor and a third switching element controlled by said voltage value at said output end and provided between said input end of said second comparator for receiving said reference voltage and either one of said first voltage supply and said second voltage supply.

9. The display apparatus as set forth in claim 8, wherein said first, second and third switching elements are MOSFETs.

10. The display apparatus as set forth in claim 9, wherein said first switching element is an N channel MOSFET and said second switching element is a P channel MOSFET.

11. The display apparatus as set forth in claim 9, wherein said third switching element is an N channel MOSFET.

12. The display apparatus as set forth in claim 7, wherein said second comparator exhibits hysteresis during operation.

13. A method of providing power, comprising the steps of:

comparing an input voltage with an output voltage;

turning on a first switching element if said output voltage exceeds said input voltage;

comparing said output voltage with a reference voltage, wherein said reference voltage can change in value between at least two different voltage values without a corresponding change in said input voltage; and

turning on a second switching element if said output voltage is lower than said reference voltage.

14. The method as set forth in claim 13, wherein said first and second switching elements are MOSFETs.

15. The method as set forth in claim 14, wherein said first switching element is an N channel MOSFET and said second switching element is a P channel MOSFET.

16. The method as set forth in claim 13, further comprising the step of turning on a third switching element if said output voltage exceeds said reference voltage.

17. The method as set forth in claim 16, wherein said first, second, and third switching elements are MOSFETs.

18. The method as set forth in claim 17, wherein said first switching element and said third switching element are N channel MOSFETs, and said second switching element is a P channel MOSFET.

19. The method as set forth in claim 13, wherein said voltage value of said reference voltage is one value when said output voltage is greater than said reference voltage and another value when said output voltage is less than said reference voltage.

20. The method as set forth in claim 13, wherein hysteresis is exhibited during said comparing of said output voltage with said reference voltage.

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